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# A Novel Architecture For An Energy Efficient And High Speed Sar Adc

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***Abstract :*** *This brief involves the design and implementation of an energy-efficient and high speed SAR ADC. The DAC would be designed to reduce the power consumption by applying a switching scheme. The architecture of SAR module provides improved speed of conversion. Power consumption is one of the main design constraints in today ICs. For systems that are powered by small non rechargeable batteries over the entire life time, such as medical implant devices low power consumption is important. In these systems SAR ADCs are key components to interface between analog world and digital domain. The design is implemented using Very High-speed Integrated Circuit Hardware Description Language (VHDL). The operations of SAR ADC are simulated using the Modelsim tool and SAR ADC design is synthesized using Xilinx tool.*
***Keywords -*** *Analog to Digital Converter (ADC), Digital to Analog Converter (DAC),), Power drawn from reference (Eref), Successive Approximation Register (SAR, Switching Energy (Esw)*

## I. Introduction

A successive approximation ADC is a type of analog-to-digital converter that converts a continuous analog waveform into a discrete digital representation via a binary search- through all possible quantization levels before finally converging upon a digital output for each conversion.
An SAR ADC is a very attractive solution for low-power analog-to-digital conversion. Here presents a highly energy-efficient switching scheme for successive approximation register (SAR) analog -to digital converters that achieves a reduction in switching energy over the conventional SAR. The highly digital nature of a SAR ADC makes it very amenable to technology scaling. Combined with low power consumption, the digital nature of a SAR ADC can exploit the benefits of the ever shrinking technology nodes. For these reasons, the SAR ADC has recently captured the attention of the research community and is increasingly being used in different applications. On one hand, medium-resolution SAR ADCs are increasingly finding use in very high sampling rate (200–500 MS/s) applications. On the other hand, low-frequency ultra-low power SAR ADCs are being used in biomedical applications and low energy radios.
In many cases, the digital-to analog converter (DAC) can contribute a significant part toward the total power consumption of the SAR ADC. This has brought to fore the challenge of further reducing the power consumption of the DAC. Unfortunately, the conventional DAC is not very power efficient, and more so if its initial guess of the input is wrong. All the switching energy reduction techniques only account for the power drawn from the reference but largely ignore the power dissipated in driving the switches. The energy spent in driving the switches can form a significant part of the overall switching energy, particularly for the highly energy-efficiency techniques. To clearly differentiate the two components of the switching energy, henceforth the switching energy drawn from the reference will be denoted by Eref and the switching energy spent on driving the switches will be denoted by Esw. The use of the proposed switching technique allows the unit capacitance to be increased by 4×compared with the conventional technique. The delay of SAR ADC can be controlled by changing the architecture of Successive Approximation Register module.

## II. Conversion Principle

The successive approximation Analog to digital converter circuit typically consists of four chief sub circuits:
1. A sample and hold circuit to acquire the input voltage (Vin).
2. An analog voltage comparator that compares Vin to the output of the internal DAC and outputs the result of the comparison to the successive approximation register (SAR).
3. A successive approximation register sub-circuit designed to supply an approximate digital code of Vin to the internal DAC.
4. An internal reference DAC that, for comparison with VREF, supplies the comparator with an analog voltage equal to the digital code output of the SAR in.

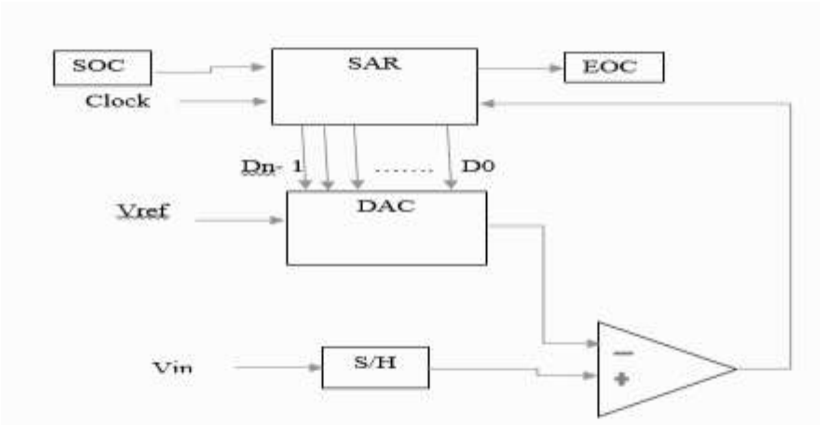



Fig. 1.1 Basic SAR ADC

DAC = Digital-to-Analog converter

EOC = end of conversion

SAR = successive approximation register

S/H = sample and hold circuit

Vin = input voltage

Vref = reference voltage

The successive approximation register is initialized so that the most significant bit (MSB) is equal to a digital 1. This code is fed into the DAC, which then supplies the analog equivalent of this digital code (Vref/2) into the comparator circuit for comparison with the sampled input voltage. If this analog voltage exceeds Vin the comparator causes the SAR to reset this bit; otherwise, the bit is left a 1. Then the next bit is set to 1 and the same test is done, continuing this binary search until every bit in the SAR has been tested. The resulting code is the digital approximation of the sampled input voltage and is finally output by the SAR at the end of the conversion (EOC).

## III. Existing scheme

In SAR ADCs, the main sources of power consumption are the DAC network, comparator, voltage reference and digital control circuit. The power consumption of the comparator and DAC capacitor networks are limited by mismatch and noise.

### 3.1 FOUR TIMES REDUCTION IN CAPACITANCE

The proposed technique can be easily generalized to a SAR ADC with any resolution. It can be seen that the proposed technique requires a total capacitance of 4 C for a 3-bit ADC compared with a 16-C total capacitance required in the conventional method. Thus, the proposed technique achieves a 4× reduction in capacitance of the DAC. The proposed scheme achieves a reduction of 4× by switching the last unit capacitor between (*V*ref, *V*cm) instead of (*V*ref,0).

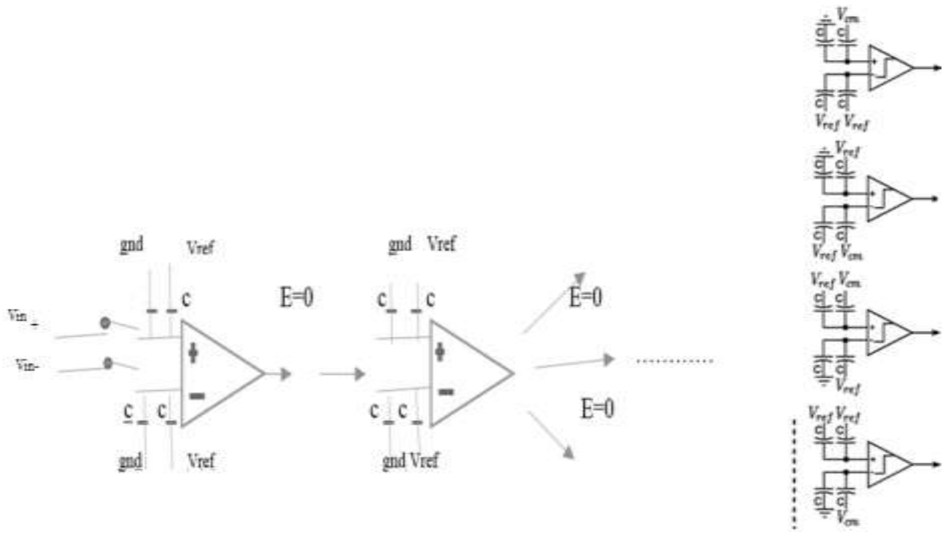



Fig 1.2 Switching scheme

This allows an additional comparison and the outputs of the comparator can be directly combined with the DAC outputs to generate the final digital code. The $V$cm value does not have to be accurate nor does its use dissipate more power. This is due to two reasons. The reference level, i.e., $V$cm, is used only for the last unit capacitor, and an error in its value does not degrade the resolution seriously.

## 3.2. ZERO SWITCHING ENERGY IN THE FIRST 2 CYCLES

The use of top-plate sampling ensures that $E$ref = 0 in the first cycle. The concept of reducing the switching energy in the second cycle is introduced in Fig 1.3. Fig.1.3 indicates the simplified initial switching sequence proposed in this brief

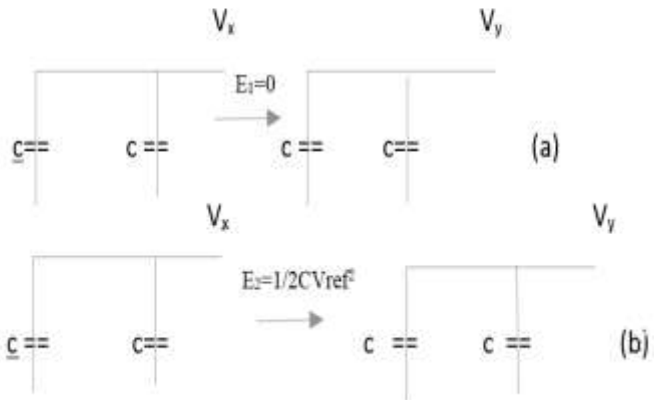



Fig 1.3 Switching energy

Applying charge conservation on Fig 1.3 (a),

$$Vy = Vx + V\text{ref}/2 \qquad (1)$$

The switching energy $E1$ can be calculated as

$$E1 = \{2(Vx - Vy) + V\text{ref}\}CV\text{ref} = 0 \qquad (2)$$

Thus, no energy is drawn from $V$ref . However, if the sequence is reversed, applying charge conservation gives

$$Vy = Vx - V\text{ref}/2 \qquad (3)$$

Hence, the switching energy $E2$ is given by

$$E2 = (Vx - Vy)CV\text{ref} = CV\,\text{ref}/2 \text{ not equals to } 0 \qquad (4)$$

*E*ref = 0, during the second cycle, as shown in Fig 1.3 Grounding the MSB capacitor initially also provides another important advantage over the monotonic switching technique in terms of the common-mode voltage variation at the comparator's inputs. The common mode variation at the comparator's inputs is given by $\Delta V$cm = *V*cmi− *V*ref/2, where *V*cmi is the common-mode voltage at the comparator's inputs. A $\Delta V$cm can cause an input-dependent offset resulting in harmonic distortion at the output.

## IV. Proposed SAR Architecture

The successive approximation register consists of a sample-and-hold (S/H) circuit, comparator, digital-to-analog converter (DAC) and logic control unit. The ADC employs a binary-search algorithm that uses the digital logic circuitry to determine the value of each bit in a sequential or successive manner based on the outcome of the comparison between the outputs of the S/H circuit and DAC feedback from array capacitances. The architecture of SAR conversional ADC, consisting of control logic unit, the SAR control includes shift register, SR latch, bit catches and buffer, the SAR works to control the DAC operation by performing the binary feedback through the successive approximation register. The SR latch detects the differential output of the comparator and holds the comparator results, bit catches perform to save result of each cycle.

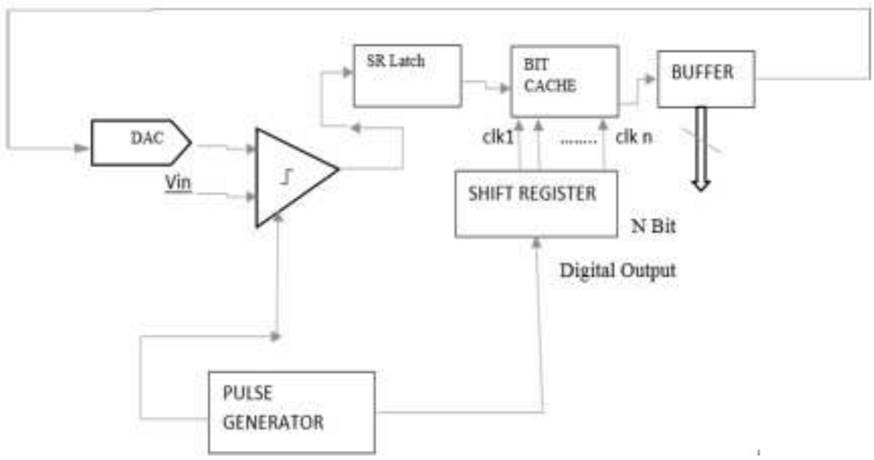



Fig 1.4 Logic diagram of SAR

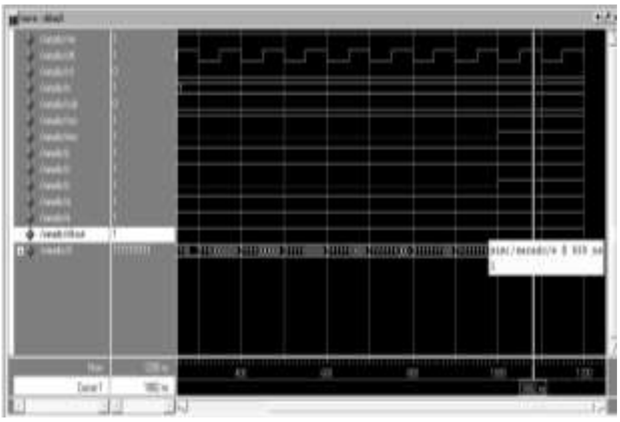
Clock pulse generates from shift register to control bit catches by turn on/off. However, the SR latch is composed of two NAND gates and bit catches composed of DFFs, both of them are sequential circuits, whose states depend on applied previously input variable as well as current inputs.

## V. ANALYSIS OF REULTS

### 5.1 .SIMULATION RESULTS

The proposed scheme ensures that only one capacitor is switched in every comparison cycle, which also helps in reducing the total switching energy. The proposed technique ensures that, for SAR ADCs with resolution less than or equal to 3 bits, the average Eref is zero for all the cycles. The negative switching energy in the last cycle is not nonphysical; rather, it implies that the DAC gives back energy to the reference voltage sources. However, for an n-bit SAR ADC, with n >3, the average Eref is nonzero and is given by,

Eref = (_n−2i=2 2n−3−i) CV2ref



*(a)*

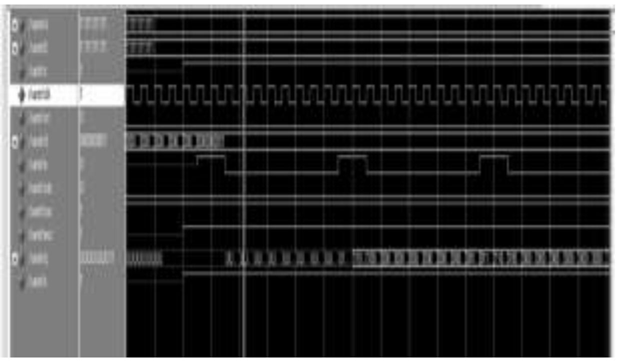
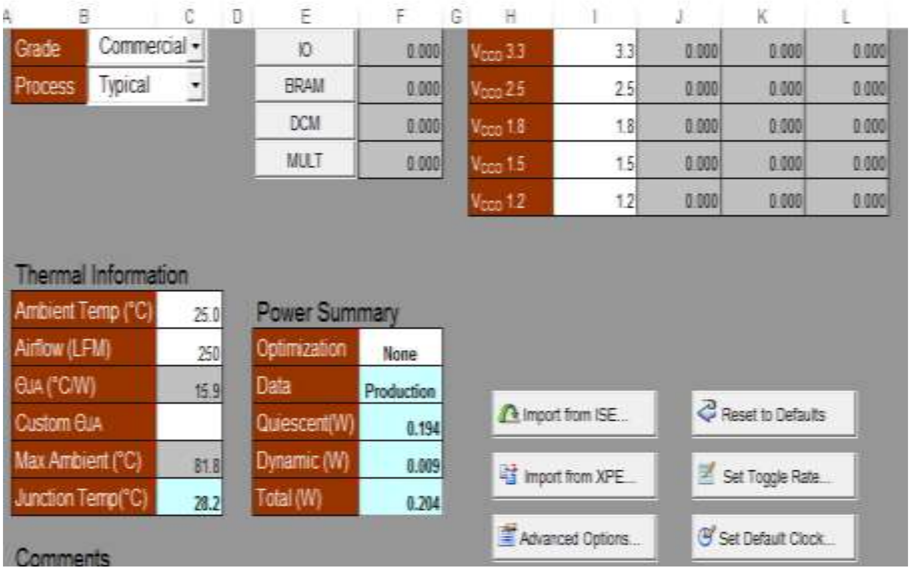


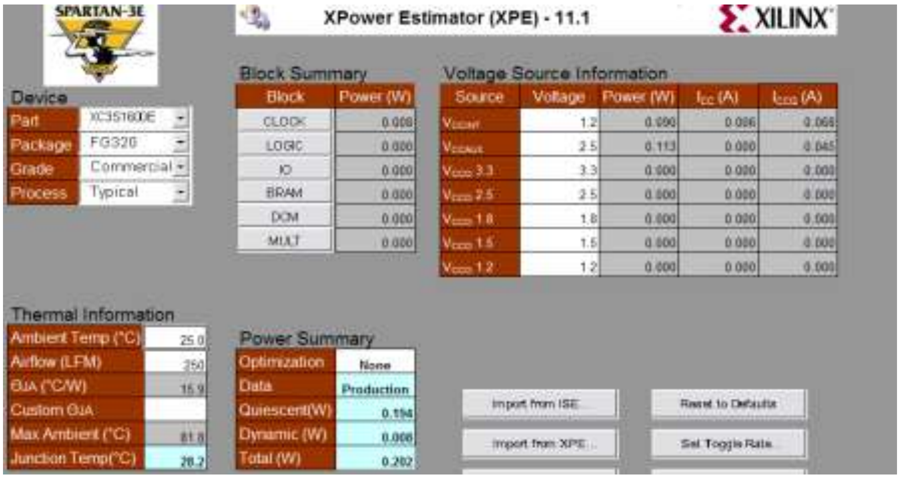
Fig1.5 Simulation results

## 5.2. POWER ANALYSIS AND COMPARISON WITH EXISTING SYSTEM

The power required for this technique is found out using XPOWER ESTIMATOR (XPE) TOOL .The figure 1.6 shows the power consumption of this technique.




(a)Applying Switching scheme only(existing system)



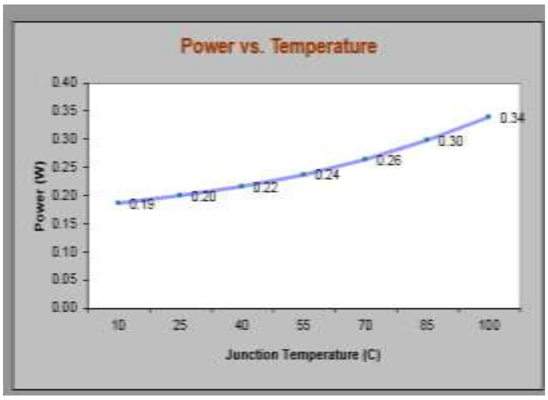

(b) Using the Proposed SAR architecture and Switching scheme

Fig 1.6 Power estimated using XPE

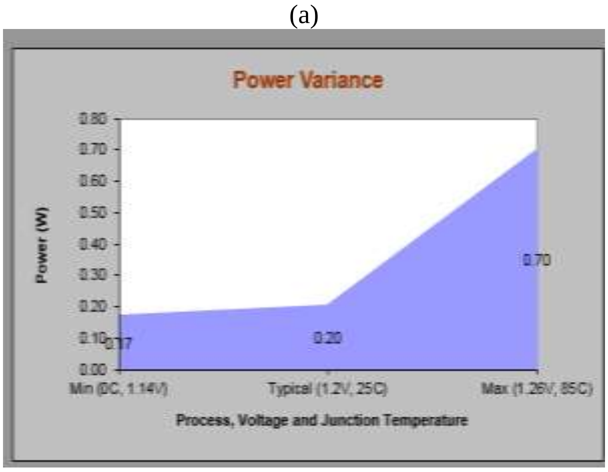
The Figure of Merit of the SAR ADC can be estimated as,

$$FoM = 0.28/2^{(10)}$$
$$= 0.273fJ/Cycle$$

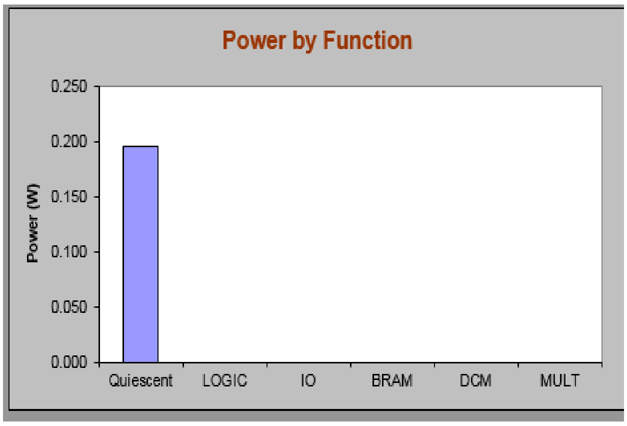
The power plots of the proposed SAR ADC is shown in figure 1.7. The fig 1.7(a) shows the variation junction temperature with power. Junction temperature is the highest operating temperature of the actual semiconductor in an electronic device. The plot explains the variation is almost linear. The junction temperature is optimum for a 0.202W power.



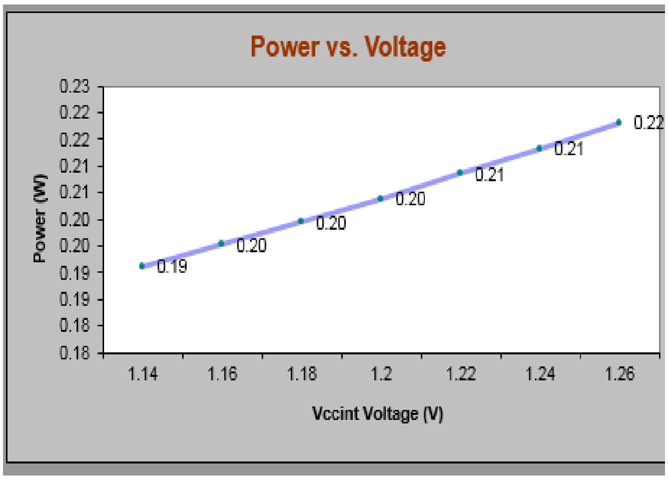

(a)




(b)




(c)




(d)

Fig 1.7 Power analysis plots

TABLE I. COMPARISON OF PROPOSED SYSTEM WITH EXISTING AND CONVENTIONAL SYSTEMS

| **SYSTEM** | **Observed Variables (n= 10 bits)** | | |
|---|---|---|---|
| | ***Energy (pJ)*** | ***FoM*** | ***Minimum Period*** |
| Conventional | 1.46 | 1.49 | 6.07ns |
| Existing System | 1.06 | 1.03 | 5.24ns |
| Proposed System | 0.89 | 0.86 | 4.25ns |

## VI. Conclusion

A highly energy-efficient switching technique for SAR ADCs has been presented in this brief and delay can also be reduced. The energy consumed by the switches has been taken into account and has been shown to degrade the overall energy savings. The proposed scheme benefits has low switching energy and improved speed compared to existing schemes.

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